ABSTRACT OF THE DISCLOSURE

A computer system comprising at least two processing sets. Each processing set includes main memory. A bridge connects the processing sets. At least a first processing set further including a dirty memory having dirty indicators for indicating dirtied blocks of the main memory of the first processing set. The bridge includes a direct memory access controller that is operable to copy blocks of the first processing set indicated in the dirty memory to the main memory of another processing set. The processors do not, therefore, need to carry out the copying, whereby the processor overhead associated therewith can be avoided, increasing the efficiency of memory reintegration. The direct memory access controller can be arranged to search the dirty memory for dirty indicators indicative of dirtied blocks. Alternatively, the dirty memory can include control logic operable to search the dirty memory for dirty indicators indicative of dirtied blocks. The direct memory access controller can be arranged to instigate a search of the dirty memory.